Then, in step S190, the modem enters the showtime. Control then continues to step S200, where the control sequence ends.

[0036] Fig. 3 outlines in greater detail the perform supplemental training block S150 in Fig. 2. In particular, control begins in step S500 and continues to S510. In step S510, the time domain equalizer coefficients are initialized. Next, in step S520, m is set to zero. Then, in step S530, the mean squared signal value is determined for each bin, for the given time domain equalizer coefficients. Note that the s_k is equal to the medley 4-QAM reference symbol in bin k multiplied by the estimated complex channel frequency response at bin k, obtained during reverb training, multiplied by a Fourier basis row vector of length L having frequency $2\pi k/m$, multiplied by the time domain equalizer coefficients (a). Control then continues to step S540.

[0037] In step S540, n is set equal to zero and the mean square error is also set to zero. Next, in steps S550 through S570, the average error squared value is evaluated, over N_1 frames, for each bin. Thus, the signal $s_k(n)$ and the received data B(n) are frame dependent. Then, in step S580, W_s and W_e will be established as diagonal matrices with elements W_k^s and W_k^e. This allows localization of linearized metrics about the current time domain equalizer coefficients. Control then continues to step S590.

[0038] In step S590, n is set equal to zero, and the matrices G_e and G_s are initialized to all-zeros matrices. Next, in steps S590 through S650, G_s and G_e, which are functions of the reference signal $u_k(n)$ and the received data B(n) for each frame, are averaged over N_2 frames. Note that $a^+\{E[G_e] - E[G_s]\}a$ is a linearized/localized approximation for

$$\sum \log_{10}(1/SNR_k)$$

[0039] which is the metric to be minimized. Then, for the next TDQ vector, the minimum Eigen vector solution is determined and the process is repeated using the updated determined localization. Control then continues to step S690 where the control sequence ends.

[0040] As illustrated in FIG. 1, the time domain equalizer coefficient determination system can be implemented either on a single program general purpose computer, or a separate program general purpose computer. However, the time domain equalizer coefficient determination system can also be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element, an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as a discrete element circuit, a programmable logic device such as a PLD, PLA, FPGA, PAL, a modem, or the like. In general, any device capable of implementing a finite state machine that is in turn capable of implementing the flowcharts can be used to implement the time domain equalizer coefficient determination system according to this invention.

[0041] Furthermore, the disclosed method may be readily implemented in software using object or object-oriented software development environments that provide source code that can be used on a variety of computer or workstation hardware platforms. Alternatively, the disclosed line time domain equalizer coefficient determination system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software and/or hardware systems or microprocessor or microcomputer systems being utilized. The time domain equalizer coefficient determination system and methods illustrated herein, however, can be readily implemented in hardware and/or software using any known or later-developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and a general basic knowledge of the computer and communications arts.

[0042] Moreover, the disclosed methods may be readily implemented as software executed on a programmed general purpose computer, a special purpose computer, a microprocessor, or the like. In these instances, the methods and systems of this invention can be implemented as a program embedded on a personal computer such as a Java® or CGI script, as a resource residing on a server or graphics workstation, as a routine

embedded in a dedicated line characterization system, a modem, a dedicated time domain equalizer coefficient determination system, or the like. The time domain equalizer coefficient determination system can also be implemented by physically incorporating the system and method into a software and/or hardware system, such as the hardware and software systems of a time domain equalizer coefficient determination system or modem, such as a DSL modem.

[0043] It is, therefore, apparent that there has been provided, in accordance with the present invention, systems and methods for determining time domain equalizer coefficients. While this invention has been described in conjunction with a number of exemplary embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, the invention is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.